REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended the independent claims in the application, that is, claims 2, 3, 9-11 and 17-19, to recite therein that the porous stress relaxing layer has a greater porosity than that of the organic protecting film. Note previously considered claim 25. In light of amendments to the independent claims, claim 25 has been cancelled without prejudice or disclaimer.

The Examiner is thanked for the indication of allowable subject matter in claim 25, set forth in Item 31 on page 7 of the Office Action mailed November 20, 2003. Also to be noted is the statement by the Examiner in Item 32 on page 7 of the Office Action mailed November 20, 2003, that "the prior art does not disclose or make obvious that the porous stress relaxing layer has a greater porosity than that of the organic protecting film including all the limitations set forth in the independent claim". Thus, as indicated by the Examiner, it is respectfully submitted that claims 2, 3 and 9, setting forth the subject matter of previously considered claim 25 in independent form, should clearly be allowed.

Moreover, as will be shown infra, it is respectfully submitted that all claims presently in the application, each reciting that the porous stress relaxing layer has a greater porosity than that of the organic protecting film, should be allowed. In this regard, by providing the porous stress relaxing layer as in the present claims, problems due to moisture and breakage, as well as problems in connection with warping, can be avoided. Moreover, using a porous stress relaxing layer which is exposed to the outside of the semiconductor device, this stress relaxing layer being used together with

an organic protecting film provided on an opposite side of the chip to that provided with the stress relaxing layer, moisture absorbed can be released outside of the package through the porous stress relaxing layer, thereby avoiding possible cracking and peeling due to, e.g., expansion of the moisture at mounting re-flow.

As for advantages according to the present invention, having, for example, relative porosity of the porous stress relaxing layer and of the organic protecting film as in the present claims, essentially where side planes of the porous stress relaxing layer are exposed to outside of the semiconductor device, especially with various structures exposed to outside of the semiconductor device on a same plane, note pages 47 and 48 of Applicants' Substitute Specification submitted with the Preliminary Amendment filed March 31, 2000, in the above-identified application.

Kim, et al. (U.S. Patent No. 6,004,867) discloses a chip-size package including a semiconductor chip having a plurality of input/output pads on an active surface thereof, and a passivation layer covering the active surface such that the input/output pads are exposed. Note particularly column 1, lines 53-65, as well as from column 1, line 67 to column 2, line 5. Note also the last paragraph in column 2, and the second paragraph in column 3, of Kim, et al. This patent discloses a passivation layer covering the active surface of the chip except for the input/output pads.

It is respectfully submitted that the passivation layer of Kim, et al., for protection purposes, would have neither disclosed nor would have suggested the porous stress relaxing layer of the present invention, much less the relative porosity of the stress relaxing layer to that of the organic protecting film as in the present invention.

It is respectfully submitted that the teachings of Ball, et al. (U.S. Patent

No. 6,351,022) would not have rectified the deficiencies of Kim, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Ball, et al. discloses a system for processing a planar structure, such as a semiconductor wafer, wherein a wafer is segmented into portions and then the thickness of the segmented portions is reduced. Note, in particular, column 2, lines 4-9. This patent discloses a protective material such as polyimide tape or polyamide coatings, being applied to the front and back surfaces of the wafer. See column 3, lines 25-32. Note also column 3, lines 39-44 disclosing removal of the front protective coating.

Even assuming, arguendo, that the teachings of Kim, et al. and Ball, et al. were properly combinable, such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including, inter alia, relative porosities of the porous stress relaxing layer and of the organic protecting layer, and advantages thereof as discussed previously.

As discussed in the following, it is respectfully submitted that the teachings of the additional references as applied by the Examiner on pages 4-6 of the Office Action mailed November 20, 2003, would not have rectified the deficiencies of the combined teachings of Kim, et al. and Ball, et al., even if such teachings were properly combinable, such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Chang, et al. (U.S. Patent No. 6,353,182) discloses packaging semiconductor devices with laminar substrates using the flip chip packaging technique, by matching the z-direction coefficient of thermal expansion (CTE) of the IC solder joint with the z-direction CTE of the encapsulant. Note column 3, lines 33-46. See also column 2, lines 48-57 and 60-62 and column 2, line 64 to column 3, line 4. Note also column 4, lines 8-12 and 48-57.

European Patent Application No. 504,669 discloses a semiconductor device which includes an integrated-circuit chip or another semiconductor element on a substrate, wherein a porous polytetrafluoroethylene (PTFE) layer is positioned between the semiconductor element and the substrate. See column 2, lines 11-33. Note also column 3, lines 33-36, and column 4, lines 39-45.

Even assuming, arguendo, that the disclosure of this European patent application were properly combinable with the disclosure of the other references as applied by the Examiner, such combined disclosures would have taught away from the present invention, having relative porosities of (1) the porous stress relaxing layer provided on the plane whereon circuits and electrodes are formed of the semiconductor chip, and (2) the organic protecting film provided on a plane opposite to the stress relaxing layer of the semiconductor chip.

Akagawa (U.S. Patent No. 6,121,688) discloses use of an anisotropic conductive sheet, having a conductive layer (see column 1, lines 40-47), and a semiconductor device having a plurality of anisotropic conductive sheets laminated on each other (see column 2, lines 43-65).

Sasaoka, et al. (U.S. Patent No. 6,010,769) discloses a multilayer wiring board and a method for manufacturing the same, including a conductive pillar connecting a first via land and a second via land, the pillar having an intruded zone in the first insulating layer through a hole of the first via land. Note column 5, lines 11-22. See also column 12, lines 15-22 and 35-37.

Japanese Patent Document No 8-262487 (Watanabe) discloses a liquid crystal display device wherein the driving IC chip 121 (note Fig. 1) is packaged not on the substrate 101 disposed with the thin film transistors but on the substrate 102 facing the substrate 101.

Hashimoto (U.S. Patent No. 6,475,896) discloses a semiconductor device having a package size close to the chip size, that includes a semiconductor chip having electrodes; a stress relieving layer provided on the semiconductor chip so as to avoid at least a part of the electrodes; wiring formed from the electrodes over the stress relieving layer; and external electrodes formed on the wiring over the stress relieving layer. Note column 5, lines 45-52. This patent further discloses that the semiconductor chip may have a protective film on the surface opposite to the surface having the electrodes. See column 6, lines 3-5. Note also column 1, line 66 to column 2, line 9; column 2, lines 39-40 and 52-56; column 4, lines 42-45; and column 6, lines 6-8.

Even assuming, arguendo, that the teachings of Hashimoto, or any of the other references applied together with the teachings of Kim, et al. and Ball, et al., were properly combinable with the teachings of Kim, et al. and Ball, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed subject matter, including, inter alia, the porous stress relaxing layer and

organic protecting film respectively provided on (1) a plane whereon circuits and electrodes of the semiconductor chip are formed, and (2) on the plane opposite to this plane where the circuits and electrodes of the semiconductor chip are formed, with relative porosity of the organic protecting film and porous stress relaxing layer, and/or other aspects of the present invention including, inter alia, where respective side planes of the stress relaxing layer, the semiconductor chip and the organic protecting film are exposed to outside of the semiconductor device on a same plane (or where side planes of the stress relaxing layer are exposed to outside of the semiconductor device).

In view of the foregoing comments and amendments, reconsideration and allowance of all claims remaining in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 503.37770X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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